R E M A R K S

Careful review and examination of the subject application are noted and appreciated. Reconsideration of the claims is respectfully requested.

INTERVIEW SUMMARY

Applicants' representative, John Ignatowski, spoke with Examiner Duncan the week beginning April 18, 2005 via telephone. Applicants' representative requested clarification how the claimed "predetermined direction" phrase in claim 1 was apparently being interpreted as both a high to low direction AND a low to high direction in the Office Action. The Examiner noted that a "predetermined direction" may be interpreted as an "opposite direction". No other claims were discussed. No samples were presented. No agreement was reached regarding the claims.

FOREIGN PRIORITY

The Office Action indicates on the PTOL-326 form that only some of the certified copies of the priority documents have been received. However, the Office Action fails to identify the certified copies allegedly not received. Therefore, the Examiner is respectfully requested to either (i) identify the missing documents or (ii) acknowledge reception of all certified copies of the priority documents.

SUPPORT FOR THE CLAIM AMENDMENTS

Support for the claim amendments may be found in the specification, for example, on page 8 lines 17-20, page 15 lines 3-5, page 15 lines 13-16, page 16 line 15 thru page 17 line 4 and FIGS. 4 and 5, as originally filed. Thus, no new matter has been added and no new issues are believed to be raised for the independent claims.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-20 under 35 U.S.C. §102(b) as being anticipated by Schenck '329 has been obviated in part by appropriate amendment, is respectfully traversed in part, and should be withdrawn.

Schenck concerns a method and system of minimizing simultaneous switching noise in an electronic device (Title).

Claim 18 provides a means for inverting a plurality of signals **only in response to** at least a predetermined number of the signals transitioning in a predetermined direction. In contrast, Schenck appears to contemplate (see column 2, lines 16-30 and column 6, lines 44-61) inverting bus signals any time a majority of the bus signals transition to either a high logic state or a low logic state. Schenck appears to be silent regarding inverting the bus signals **only in response to** the signals transitioning in a predetermined direction, for example high to low. Furthermore, the

Office Action admits on page 2 last line thru page 3 first line that Schenck discloses complementing (inverting) the bus signals "when more than half of the data lines need to be switched from high to low **or** low to high." (Emphasis added) Therefore, Schenck does not appear to disclose or suggest a means for inverting a plurality of signals only in response to at least a predetermined number of the signals transitioning in a predetermined direction as presently claimed.

Assuming, *arguendo*, that the claimed "predetermined direction" may be similar to an "opposite direction" from a current logic state to an opposite logic state (for which Applicants' representative does not necessarily agree), the interpretation of the claim language would appear to violate MPEP §2111. MPEP §2111 states:

> During patent examiner, the pending claims must be "given their broadest reasonable interpretation consistent with the specification." *In re Hyatt*, 211 F.3d 1367, 1372, 54 USPQ2d 1664m 1667 (Fed. Cir. 2000) . . . The broadest reasonable interpretation of the claims must also be consistent with the interpretation that those skilled in the art would reach. *In re Cortright*, 165 F.3d 1353, 1359, 48 USPQ2d 1464, 1468 (Fed. Cir. 1999).

Interpreting the claim language so broadly that a "predetermined direction" could be read as both a low to high direction and a high to low direction in a single embodiment appears to conflict with the specification page 8 line 17 thru page 9 line 1. In particular, the specification states that a monitoring circuit "(ii) counts the number of data signals simultaneously switching

from a first to a second state..." Applicants teach monitoring for transitions from a first state to a second state (e.g., a transition in a predetermined direction), not monitoring for transitions away from whatever current logic state the signal is in. Therefore, the broad "opposite direction" interpretation appears to be inconsistent relative to the specification.

Furthermore, the "opposite direction" interpretation would appear to be inconsistent with how one skilled in the art would likely understand the claim language. Claim 18 provides a means for monitoring the signals for transitions. One of ordinary skill would appear to understand each monitored transition of a signal to be a change away from a current logic state. Otherwise, the signal remains at the current logic state and no transition takes place. Furthermore, one of ordinary skill in the art would appear to understand the phrase "in a predetermined direction" to provide some further limitation on the claimed transition. In contrast, the "opposite direction" interpretation appears to be so broad that the claimed phrase "in a predetermined direction" has the same meaning as a transition and is thus redundant to the "transition" claim language. The broad "opposite direction" interpretation would thus appear to be inconsistent with the interpretation by one skilled in the art expecting the phase "in a predetermined direction" to have some meaning limiting a transition. Therefore, the broad "opposite direction"

interpretation appears to be improper relative to one of skill in the art. As such, claim 18 is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 19 provides (from claim 18) a means for inverting the signals **only in response to** at least a predetermined number of the signals transitioning in (from claim 19) **one of** (i) a high to low direction and (ii) a low to high direction. As noted above for claim 18, Schenck appears to disclose that the bus signals are inverted **regardless** of the high to low or low to high transition direction. Schenck appears to perform an inversion of the bus signals expressly forbidden by the claim language. Therefore, Schenck does not appear to disclose or suggest a means for inverting the signals only in response to at least a predetermined number of the signals transitioning in one of (i) a high to low direction and (ii) a low to high direction as presently claimed.

Furthermore, assuming *arguendo*, that the "opposite direction" interpretation of the claimed "predetermined direction" is somehow correct (for which Applicants' representative does not necessarily agree), the Office Action fails to establish a *prima facie* case for claim 19 where the predetermined direction is one of (i) a high to low direction and (ii) a low to high direction. If the transition directions of Schenck anticipate the high to low and/or low to high transitions of claim 19, then the same transition directions of Schenck do not appear to anticipate the

"only in response to ... a predetermined direction" of claim 18. If the "opposite direction" interpretation from the telephone interview anticipates the claimed "predetermined direction", then the same "opposite direction" interpretation does not appear to anticipate either of the high to low direction or the low to high direction of claim 19. As such, claim 19 is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 20 provides a means for presenting a plurality of transition signals on a plurality of independent lines, each of the transition signals indicating a transition direction of one of a plurality of signals. In contrast, Schenck appears to contemplate that XOR gates 46 (asserted source of signals similar to the claimed transition signals) all appear to drive a single line. Furthermore, the single line does not appear to indicate a transition direction. In particular, the XOR gates 46 can only indicate if its two inputs are the same or different. The outputs of the XOR gates 46 do not appear to be able to indicate a direction of the transition between the two inputs. Therefore Schenck does not appear to disclose or suggest a means for presenting a plurality of transition signals on a plurality of independent lines, each of the transition signals indicating a transition direction of one of a plurality of signals as presently claimed. As such, claim 20 is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 1 provides a circuit configured to invert a plurality of signals **only** when at least a predetermined number of the signals transition **to a particular logic state**. In contrast, Schenck appears to contemplate (see column 2, lines 16-30 and column 6, lines 44-61) inverting bus signals any time a majority of the bus signals transition to either a high logic state **or** a low logic state. Therefore, Schenck does not disclose or suggest inverting a plurality of signals only when at least a predetermined number of the signals transition to a particular logic state as presently claimed. Claim 10 provides language similar to claim 1. As such, the claims 1 and 10 are fully patentable over the cited reference and the rejection should be withdrawn.

Claim 2 provides (from claim 1) a circuit configured to invert a plurality of signals **only** when at least a predetermined number of the signals transition to (from claim 2) **one** of (i) a high logic state and (ii) a low logic state. As noted above for claim 1, Schenck appears to contemplate inverting bus signals regardless of which logic state (high or low) the majority of the signals transition to. Schenck appears to perform an inversion of the bus signals expressly forbidden by the claim language. Therefore, Schenck does not appear to disclose or suggest a circuit configured to invert a plurality of signals only when at least a predetermined number of the signals transition to one of (i) a high logic state and (ii) a low logic state as presently claimed. Claim

11 provides language similar to claim 2. As such, claims 2 and 11 are fully patentable over the cited reference and the rejection should be withdrawn.

Claim 4 provides a transition checker circuit (i) directly receiving a plurality of signals and configured to present (ii) a plurality of transition signals each (iii) indicating a transition direction of one of the signals. In contrast, (i) the XOR gates 46 of Schenck do not appear to directly receive the signals entered into the system 10. Furthermore, (ii) Schenck appears to contemplate that the XOR gates 46 generate **a single signal** controlling a buffer 60. Furthermore, (iii) the single signal generated by the XOR gates 46 of Schenck do not appear to indicate **a transition direction**. Claim 13 provides language similar to items (ii) and (iii) above for claim 4. As such, claims 4 and 13 are fully patentable over the cited reference and the rejection should be withdrawn.

Claim 6 provides a plurality of flip-flops directly receiving the signals. In contrast, the flip-flops 42 of Schenck do not appear to directly receive the signals entered into the system 10. As such, claim 6 is fully patentable over the cited reference and the rejection should be withdrawn.

Claim 9 provides (from claim 7) a plurality of first flip-flops and (from claim 9) a plurality of second flip-flops. In contrast, the Office Action appears to be citing the same

flip-flops 42 of Schenck as both the claimed first flip-flops and the claimed second flip-flops. One of ordinary skill in the art would not appear to understand a single set of flip-flops anticipating two different sets of flip-flops. Therefore, Schenck does not appear to disclose or suggest a plurality of first flip-flops and a plurality of second flip-flops as presently claimed. Likewise, the Office Action appears to be simultaneously pointing to the same flip-flops 42 of Schenck for both the claimed sampling and claimed storing from claim 16 (through dependency from claim 15). As such, claims 9 and 16 are fully patentable over the cited reference and the rejection should be withdrawn.

Claims 3, 7, 8, 12, 14, 15 and 17 depend either directly or indirectly from independent claims 1 and 10, which are now believed to be allowable. As such, claims 3, 7, 8, 12, 14, 15 and 17 are fully patentable over the cited reference and the rejection should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

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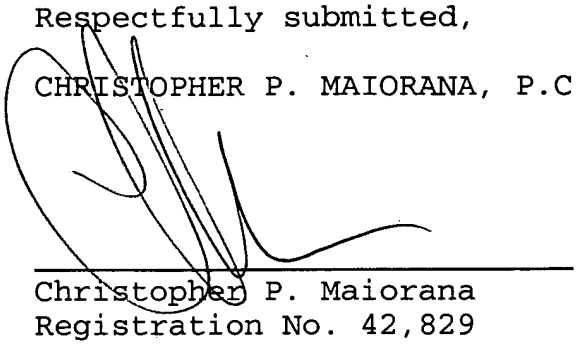

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